

Sequentially Companded Modulation for Low-Clock-Rate Speech Codec Applications

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The expansion of the step size of a speech codec may be arranged to change as the number of identical consecutive bits starts to increase. This technique causes the codec to respond partially to a fewer number of identical consecutive bits and more dramatically to larger numbers. In contrast to a typical exponential expansion of the step size, the proposed technique, in addition, expands the exponent. For speech, two distinct advantages have been observed: (i) the improvement of higher frequency audio frequency response at the same clock rate and (ii) the reduction of idle channel noise. In practice we have found that three- and four-bit companding will suffice for a typical 24 kHz, ADM codec. The proposed companding appears to be an acceptable choice between two-, three-, and four-bit companding which leads to better frequency response but worse noise, and four-bit companding which leads to both worse frequency and noise responses.

I. INTRODUCTION

The many distinct advantages of companding to encompass the dynamic range of speech signals are well documented. In most cases, a simple law is used repeatedly to arrive at the companded step size. For instance, in the 37.7 kHz, ADM SLC-40 codec,¹ a nonlinear function of the frequency of occurrence of four identical consecutive bits forces an expansion of the step size. In the two-bit companding described in Ref. 2, the expansion of step size follows a geometric progression. Three bit companding described in Ref. 3, again depends on a base-two geometric series for increasing the step size, when two consecutive bits are the same, and again on the same series with a base-half for decreasing the step size when the bits are of opposite polarity. Most of these systems perform adequately at higher (typically above 32 kHz) clock rates. However, when the clock rate is decreased, the simple fixed rules of companding either offer an unacceptable quantization noise at lower step sizes, or make the

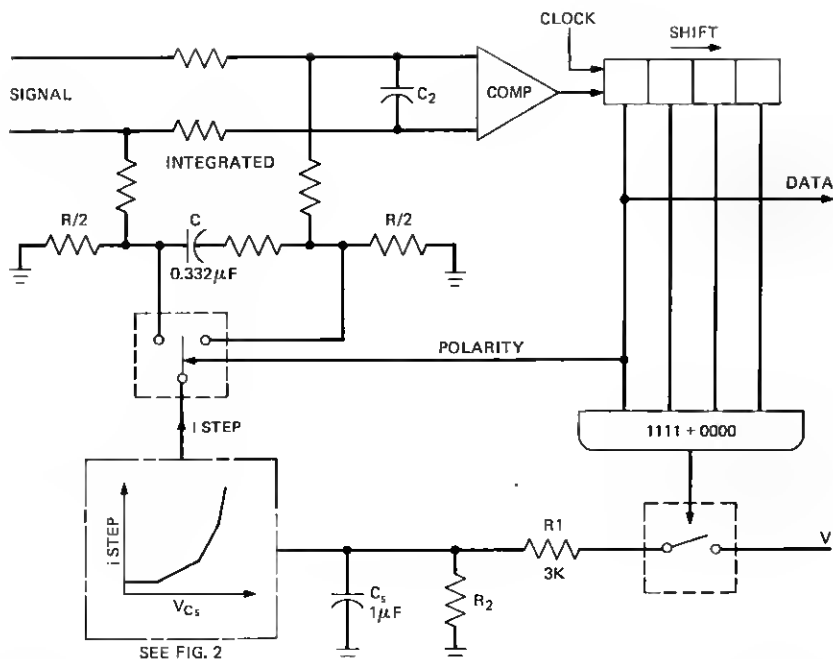


Fig. 1—Block diagram of encoder (see Ref. 4, Fig. 7).

message so choppy at larger step sizes that it becomes unintelligible. A happy compromise between the two is simply impossible. For this reason, we have investigated the problem by having a series of weightings attached to identical consecutive bit patterns of two, three, and four bits. When the bit pattern reverses, the decay of the step size is effected by an RC circuit with a time constant of about 9 msec.

Sequential companding proposes to utilize the binary sequence of data for companding the step size in a multiplicity of modes at different instants of time in a gradual way, whereas conventional encoding translates the companding information more drastically after a critical threshold has been reached. The multiple use of bit stream to convey companding information enhances the effective usage of bits at the same bit rate, or achieves the same quality of speech at a lower bit rate.

II. PERIPHERAL CIRCUIT FOR TESTING SEQUENTIAL COMPANDING

An existing ADM codec¹ has been used to test the principle of sequential companding. The encoder has a double integration feedback loop with the main pole at 235 Hz and the secondary pole at 2870 Hz. Figure 1 is a block diagram of the encoder. Four bit companding is effected by a logic circuit which forces an incremental charge on a 1 μF capacitor through a 3 k Ω resistance. The duration for which the charging

takes place equals the time during which the logic circuitry senses four consecutive ones or zeros at the output of the comparator, which in turn senses the difference between the incoming speech signal and the voltage across the feedback loop. When the four bits sensed are not all identical, the $1\text{ }\mu\text{F}$ capacitor is allowed to discharge to a $9\text{ k}\Omega$ resistance. This combination yields two time constants; one for charging (attack) of about 3 msec, and one for a discharging (decay) of about 9 msec. The voltage across the $1\text{ }\mu\text{F}$ capacitor dictates the step size. A nonlinear circuit generates a step current whose magnitude depends upon the voltage across

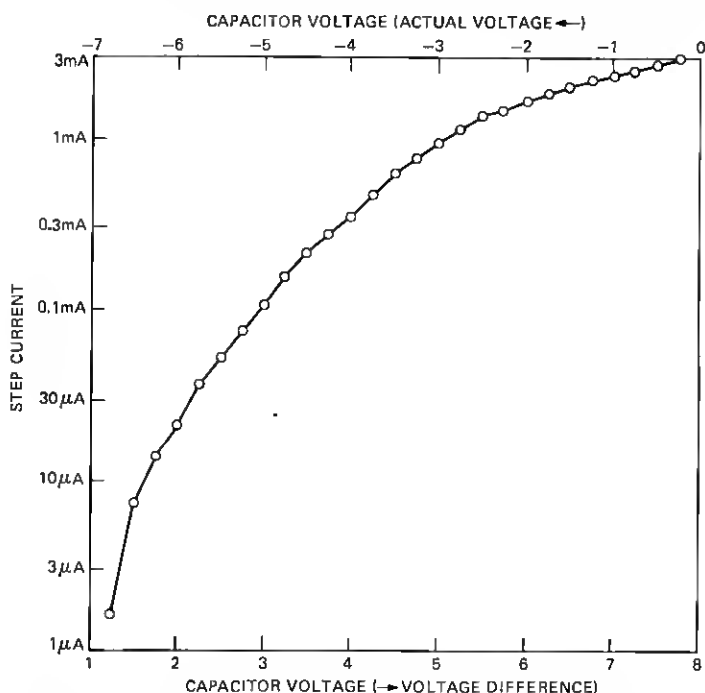


Fig. 2—Compander capacitor voltage and step current relationship.

the $1\text{ }\mu\text{F}$ capacitor. Figure 2 depicts the $1\text{ }\mu\text{F}$ capacitor voltage and the compander current. When there is no companding at all, the voltage across the capacitor becomes quite low (about 1.6 V) and the minimum step size of the $10\text{ }\mu\text{A}$ is reached. As the voltage reaches about 6.5 volts, the current step size reaches about 2 mA yielding about 46 dB range for the step size. The compander current is used to accumulate or deplete a charge on a final $0.33\text{ }\mu\text{F}$ integrator capacitor and it is the voltage across this capacitor which yields the original voice frequency signal after a low pass filter with a 3 dB loss at about 2000 Hz. The final capacitor has

about 1.2 k Ω in its discharge path. When the current step size is about 10 μ A, the voltage swings between ± 0.58 mV across the integrator capacitor at a clock frequency of 24 kHz.

III. ESSENTIAL DIFFERENCES BETWEEN CONVENTIONALLY COMPANDED AND SEQUENTIALLY COMPANDED CODECS

3.1 *The idle channel noise*

The character of the idle channel noise is totally different in the sequentially companded codecs. Whereas in the conventionally companded encoder, the bit pattern generated by the encoder during a silent period is nondeterministic and depends on the comparator characteristics, the sequentially companded encoder generates a sort of restless limit cycle in which the climax occurs when the three consecutive ones are produced, and the step size increases very slightly followed by pairs of zeros and pairs of ones for a few cycles. Meanwhile, the step size starts to decay due to lack of any companding, the paired zero-ones gradually vanish to a single zero and one combination and then the whole cycle repeats. This constitutes a semistable limit cycle and has been photographed in Figure 3a. The top trace shows the audio output from the decoder. The central trace is the integrator voltage in the decoder. The last trace is the clock at 24 kHz which also triggers the oscilloscopic sweep. In contrast a similar oscillogram (Fig. 3b) for a conventionally companded codec shows a total absence of any pattern during the silence.

These two pictures also forecast the difference in character of the two idle channel noises. The sequentially companded decoder presents a component of frequency at about 190–200 Hz which is considerably quieter than random noise generated by the conventionally companded ADM. But the higher frequency channel noises are less than those in the conventionally companded ADM coded. Psychologically the effect of such a low-frequency steady low-level signal appears to be more tolerable than the randomly varying noise produced by the latter.

Sequentially companded codecs also have one additional feature to enhance the signal to idle channel noise ratio. The frequency of companding in the three and four bit compander is higher than that in the four bit compander alone. Hence, the signal strength at the input to encoder can be higher at the same input frequency. The study of the four bit conventional codec suggests a 60 mV occasional peak at the input level to the codec. This value is appropriate and is consistent with an average voltage across to the integrator capacitor with the compander switch being functional (Ref. 4) for about 10 percent of the time. However, for a sequentially companded codec, the compander switch would be functional almost twice as frequently. However, the charging rate of

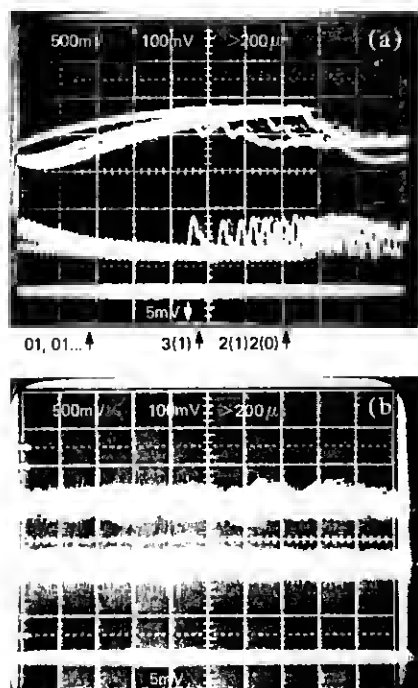


Fig. 3—Idle channel noise characteristics of (a) sequentially companded ADM codec and (b) conventionally companded ADM codecs.

the three bit compander is less than the charging rate of the four bit compander. Further, the switch for the four bit works in unison with the three bit switch. Hence, the average signal level for the sequentially companded codec tends to be on the order of 160–220 mV. At this level the sequentially companded codec at 24 kHz “sees” a frequency of 4 kHz the same way as a conventionally companded codec at 37.7 kHz would see a frequency of 4.7 kHz. But since the resistances in the charging paths are different, the responses would also be slightly different. Further, the response to the lower frequency from the sequentially companded codec should become nominally better* since both three- and four-bit companding can take place simultaneously.

The signal to noise implication of this difference of behavior between the two codecs is that whereas the noise remains about the same for the sequentially companded codec, the signal level increases about two to three times bringing down the signal to idle channel noise ratio considerably. This result has to be observed consistently during normal functioning of the codec.

* Experimentally we have seen very little difference at low audio frequencies which tend to pass through the telephone network.

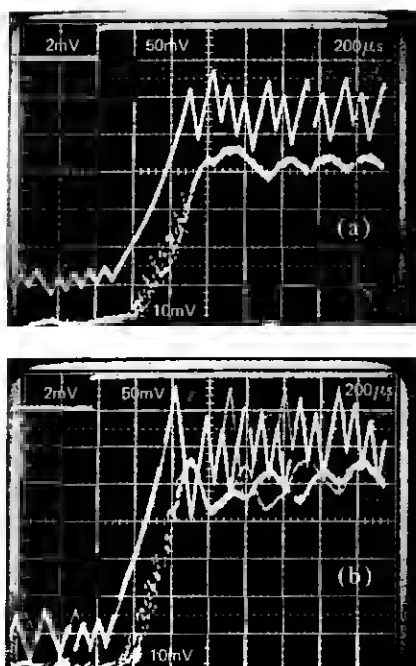


Fig. 4—Unit function response of (a) conventionally companded codec and (b) sequentially companded codec for a 50 mV step function.

3.2 Unit function response

This response indicates the rapidity with which the codec can respond to changes in the input level. It also brings about the high frequency response of the codec. During the normal operation the capacity of the sequentially companded codec to respond rapidly is reflected by lower slope overload noise. When a 50 mV step is imposed on the encoder, the decoder responses for the conventionally and sequentially companded codecs are presented in Figures 4a and b and output voltages are also tabulated in Table 1A. Similar response to a 360 mV surge is shown in Figs. 5a and b and the output voltages are presented in Table 1B.

3.3 Higher audio frequency response

An audio frequency of 3149 Hz (nonsynchronous with the 24 kHz clock) is chosen for the comparison of performance of the two codecs. Figures 6a and b represent two spectrograms generated at the output. In the response from the conventionally companded codec (Fig. 6a), the peak at the input frequency is surrounded by a large number of cluttered peaks with rapidly changing (indicated by the density of broken patterns and smears in the figure) tones. Each smear is an audible change in tone

Table IA — Differences in responses to 50 mV step function at encoder

Elapsed time, μ sec	Conventionally companded codec, mV	Sequentially companded codec, mV
200	2.5	3.0
300	10.0	15.0
400	20.0	29.0
500	32.0	47.0
600	43.5	55.5
800	44.0	48.0
1000	44.0	50.0

Table IB — Differences in responses to 360 mV step function at encoder

160	19	35
320	50	80
480	110	180
640	205	300
800	320	370
960	320	370

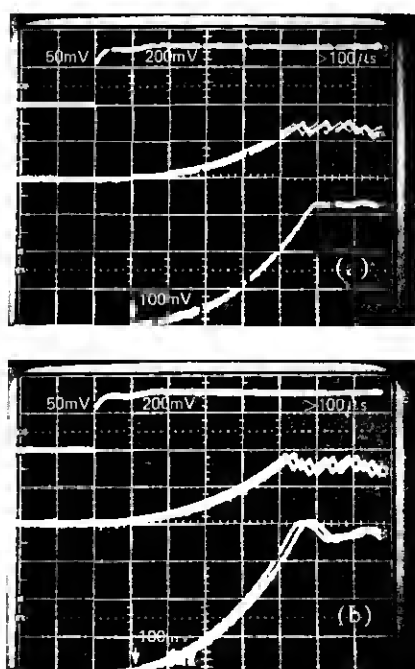


Fig. 5—Unit function responses of (a) conventionally companded and (b) sequentially companded codecs for a 360 mV input surge.

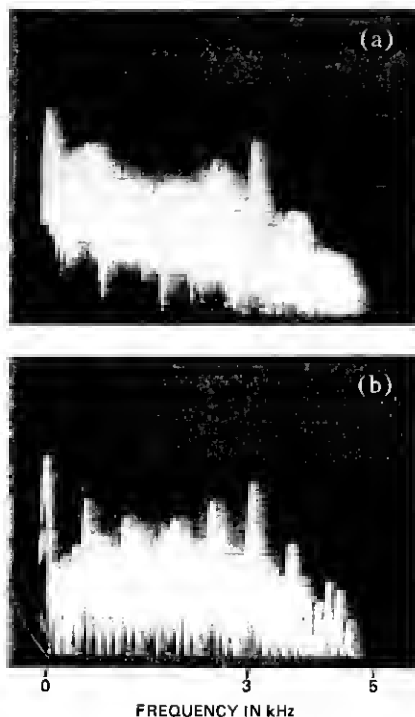


Fig. 6—Typical responses at about 3000 Hz from (a) conventionally companded and (b) sequentially companded ADM codes.

which cannot be missed by a listener. In contrast the response from the sequentially companded codec is cleaner and better formed with a fewer number of breaks and smears. Listening to the output tones from the two codecs also confirms this result.

IV. COMPUTED SIGNAL-TO-NOISE RATIOS

4.1 *Validation of the computer model*

Computerized models of the conventionally and sequentially companded codecs have been developed to compute the S/N ratios. The model of the codec programmed for a Nova 800 minicomputer is a general purpose version of a typical ADM codec whose companding can be changed by input variables. The same model serves to compute the binary sequence, the output wave shapes, the signal to noise ratios, etc., by altering the data to the minicomputer in a conversational mode of communication between the operator and the machine. For the encoder model an ideal comparator is used. Hence, the additional noise generated by the imperfection of the comparator is absent from the computed re-

Table II — Computed and measured S/N ratios

Frequency	Measured* (Ref. 4), dB	Computed,* dB
300	38.5	40.0
800	32.5	32.5
1600	22.5	22.0

* The clock rate is 37.7 kHz.

Table III — 24 kHz steady-state S/N ratios

Audio frequency, Hz*	Conventional companding		Sequential companding	
	Bits	S/N	Bits	S/N
2900	3	7.9		
	4†	5.7	3, 4	8.35
2490	3	3.7		
	4†	2.1	3, 4	3.9
1660	3	16.0		
	4†	13.0	3, 4	15.3
830	3	25.1		
	4†	23.2	3, 4	29.4
415	3	31.6		
	4†	31.0	3, 4	31.8

* These numbers are chosen to be irrational fractions of the clock rate at 24 kHz to avoid a limit cycle condition.

† Presently used charging resistance = 3.01 kΩ.

sults. This leads to the assertion that the computed S/N ratios would be the upper bound for the measured S/N ratio. These values (published in Ref. 4) have been used to validate the model at different sine wave inputs and have been presented in Table II.

From the computational models it also becomes evident that the S/N ratio is by no means a constant but a time varying quantity. Whereas the S/N ratio is measured as a time-average over a period (typically between 0.5 to 3 seconds), the computed S/N ratios are averaged over much shorter intervals and, hence, one would expect some difference between the computed and the measured values. Nonetheless, since the time constant is the same for all computations, the cross comparison of the computed values would still be a valid relative measure of their performances. To reduce the effect of transient variations of the S/N ratios, the computed value is the average of 60 such ratios at 60 consecutive clock cycles, each ratio being calculated as the moving average of twenty adjoining ratios around each clock cycle. Further, a series of such computations are made over numerous input frequency cycles and an average number is derived.

4.2 Effect of sequential companding on steady-state sinusoidal inputs

Table III lists the values of computed signal-to-noise ratios for conventionally companded and sequentially companded codecs at 24 kHz.

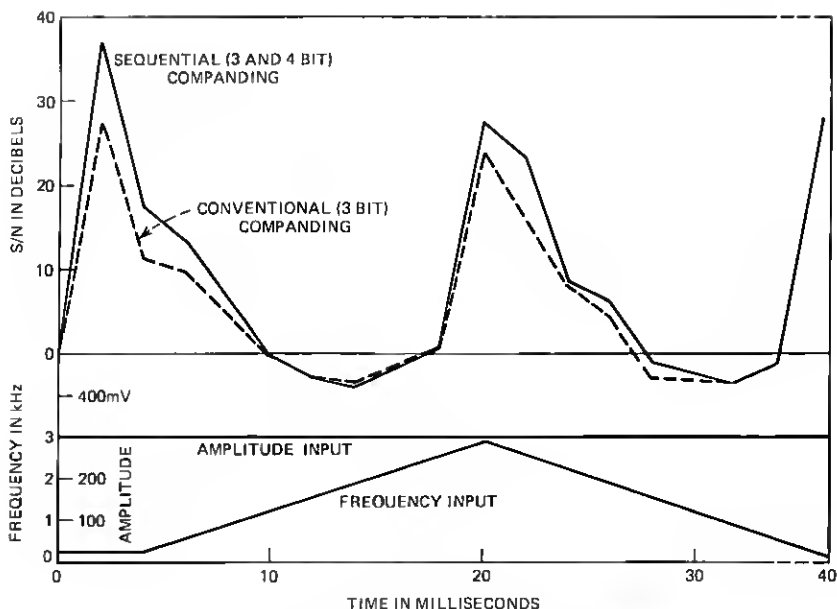


Fig. 7— S/N ratios for rapidly varying frequencies.

The input parameters have been held substantially the same for all the cases presented. However, the values of the charging resistances* for three-bit companding has been computationally optimized as 5.2 k Ω , whereas its corresponding value for four-bit companding has been retained as 3.01 k Ω as it exists in current applications. In case of the sequential companding their values† have been optimized as 5.2 k Ω for three bits and 4.36 k Ω for four bits, even though any other resistance values in their proximities will perform adequately.

4.3 Effects of sequential companding on frequency modulated sine wave Inputs

Steady tones are rarely encountered in telephone conversations. Rapidly varying frequencies are, however, typical and for this reason we have studied the responses of conventional and sequential coding at 24 kHz clock rate when the input signal has a frequency which changes gradually from 250 Hz to 2900 Hz and back to 250 Hz within 30–50 milliseconds. Such changes are well perceived by the listener and the average signal to noise ratios indicate the relative faithfulness with which

* This charging resistance controls the voltage on the step size capacitor, which in turn controls the current step for charging or depleting the final integrator.

† Experimental determination (Section III) for best subjective listening seems to indicate that 5.2 k Ω and 3.01 k Ω are the desirable values for three- and four-bit companding.

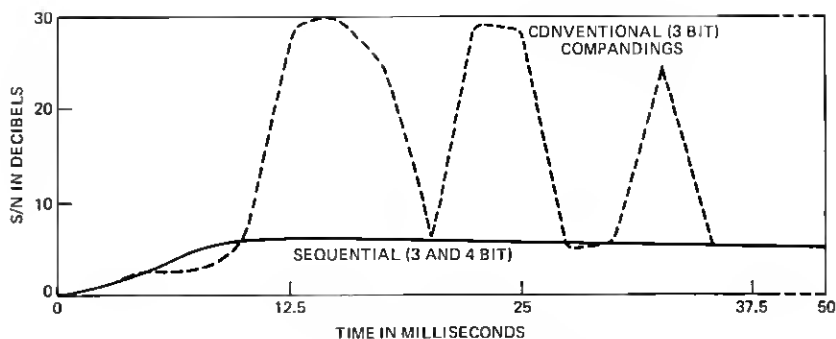


Fig. 8—Square-wave response to 1660 Hz signal.

the codecs can follow the change in frequencies and thus retain the original message characteristics.

The response to such a frequency characteristic is presented in Fig. 7. The average S/N ratio during the entire cycle is 10.18 dB for the sequential and 8.29 dB for the conventional encoding. The averages of positive S/N ratios are 17.95 dB for sequential and 14.91 dB for conventional encoding.

To signify the uneven behavior of the conventional encoding further, square wave at 1660 Hz was presented at the encoder. The results are shown in Fig. 8. The effectiveness of the sequential companding in following rapidly changing input is also illustrated in Fig. 9. Computed S/N ratios are plotted when a tone burst signal at 1660 Hz is presented to the two types of the encoders. To meet the rapidity of response of the three- and four-bit companding, the charging resistance (see Sec. 4.2) of the

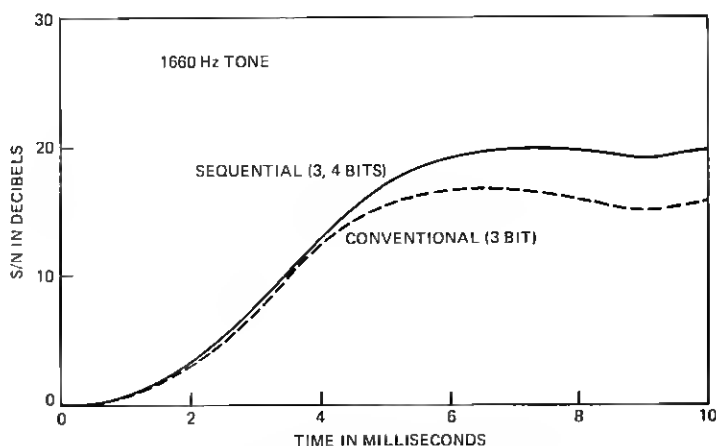


Fig. 9—1660 Hz tone burst response.

three-bit conventional companding is adjusted from 5.2 k Ω to 4.5 k Ω . However, the steady-state S/N ratio attained by the three- and four-bit sequential companding is about 18.7 dB as against 16.3 dB for the conventional companding. We have not been successful in achieving a rapid response and also a consistently high steady state S/N ratio from conventional companding to match the performance of the sequential companding. To quantify this assertion we have roughly the same rapidity of response from both codings at 830 Hz. However, the steady-state S/N ratio of sequential coding is 4.3 (29.4 vs. 25.1) dB higher than conventional coding. Complementarily, when the steady-state S/N ratios are approximately the same at 250 Hz, the sequential companding S/N ratio is roughly 9.5 (37.0 vs. 27.5) dB better than conventional companding S/N ratio 2.3 msec after the tone burst.

V. DISCUSSION OF THE DIFFERENCES

5.1 Experimental results

Consider an ideal case where a series of ones is presented at the input data of the ADM decoder. The integrator voltage responds to an increasing step current. If the discharge of this integrator capacitor is ignored for the present, then the voltage across the integrator is directly proportional to the increasing current step. Qualitatively this voltage may be represented by curves A-E of Fig. 10. At 48 kHz the change in step size after the eighth "one" is $h'i'$, whereas the step size after the fourth "one" at 24 kHz (corresponding to the same lapsed interval of time) is only hj . If the codec had three- and four-bit companding, the change in integrator voltage would have been $h''j''$ which is greater than hj due to two reasons: (i) the additional companding step at d and (ii) the simultaneous action of both the three- and four-bit companding at f'' . A simple three-bit companding would have had a slower response as depicted by the curve D.

Again consider the influence of the resistances in charging paths of the step size capacitor if there are two resistances R_1 and R' in the charging paths energized by the three-bit and four-bit companding, then the slope of the curve B can be adjusted to any desired value. Different values of these resistances yield different ranges of these curves with one essential, vital difference. When the resistance is too low, the step size becomes too coarse leading to crackle within the word every time the polarity of a bit changes after a series of ones or zeros, and it is this direction in which a real compromise must be sought while adjusting the value of the resistances to minimize the slope overload noise.

In essence, the sequentially companded ADM codec behavior differs from that of a conventionally companded codec to the extent that an additional factor of nonlinearity is imposed in its response. The con-

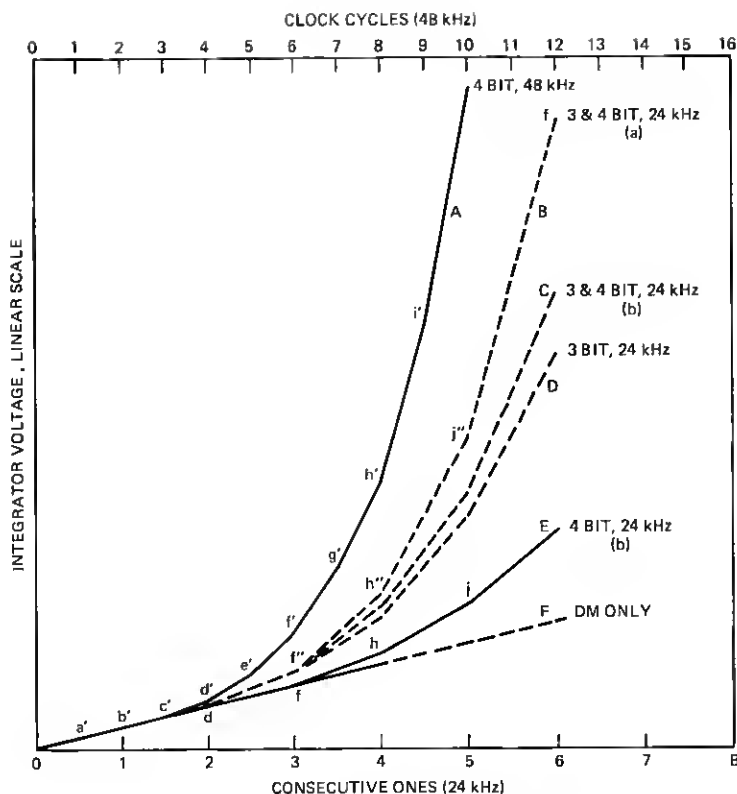


Fig. 10—Idealized responses of ADM codecs.

ventionally companded ADM codec responds by the inherent nonlinearity between the step size capacitor voltage and the current step, whereas the sequentially companded codec expands the step size capacitor voltage itself with a nonlinear character, and this nonlinearity rides along the nonlinear relation of Fig. 2 at all sizes of the current steps making the codec more responsive and more sensitive especially at lower clock rates. The validity of this assertion is demonstrated in experimental results in Figs. 4, 5, and 6.

5.2 Computational results

The steady-state sinusoidal response of a sequentially companded codec can be matched by a conventionally companded codec operating at a lower number of bits of the sequentially companded codec. However, the rapidity of such a response cannot be achieved by conventional companding which can also yield a consistently higher steady state S/N ratio. The computational verification of this assertion is indicated in Fig.

9 due to consistently lower S/N ratio from the conventionally companded codec during the cycle of frequency variation. This characteristic is reflected by crisper sounding words from sequentially companded codecs.

Sequentially companded codecs seem to reach and hold a steady state more quickly and more effectively as shown in Fig. 8. The large swing of the S/N ratio when reaching the steady state by the conventionally companded codec indicates its inadequacy to yield steady tones essential for MFKP system and *TOUCH-TONE*® signals.

VI. CONCLUSIONS

Both experimental and computational results confirm that sequential companding reduces the response time from the codec even though conventionally companded codecs can compete well in the steady state response for sine wave excitations. Further, the tones generated from sequentially companded codecs tend to have fewer breaks and thus are steadier and yield higher S/N ratios at higher audio frequencies.

Experimental results indicate that the idle channel noise from sequentially companded codecs is considerably lower than the idle channel noise from conventionally companded codecs during actual message transmission. The intelligibility of the message is also better due to crisply formed words and lower background noise.

Computational results indicate that when the frequency centers around 800 Hz and when a small frequency modulation is embedded, then the S/N ratio from the sequentially companded codecs is about 2-3 dB better than an optimally designed conventional codec.

VII. ACKNOWLEDGMENT

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REFERENCES

1. S. J. Brodin and G. E. Harrington, "The SLC-40 Digital Carrier Subscriber System," IEEE Intercon Conference Record 1975, 81, pp. 1-5.
2. N. S. Jayant, "Adaptive Delta Modulation with 1 bit Memory," B.S.T.J., 49, No. 3 (March 1970), pp. 321-342.
3. M. R. Winkler, "High Information Delta Modulation" IEEE Intl. Conv. Rec., 11, No. 8, 1963, pp. 260-265.
4. R. J. Canniff, "Signal Processing in SLC-40, a 40 Channel Rules Subscriber Carrier," ICC 75 Conference Record, Vol. 3, pp. 40-7 to 40-11.
5. S. V. Ahamed, "The Nature and Use of Limit Cycles in Stabilizing the Behavior of Semideterministic Systems," internal Bell System communication.
6. Bell Telephone Laboratories, "Transmission Systems for Communications," fourth edition, Western Electric Company, Inc., Winston Salem, North Carolina, February 1970.